Amendments to the Claims:

This listing of claims will replace all prior versions and listing, of claims in the application:

Listing of Claims:

Claims 1-3 (canceled)

Claim 4 (currently amended): A multilayer wiring structure for semiconductor devices, [according to Claim 2,] comprising:

a semiconductor substrate;

at least one active region supplied with an electric power from a power-supply potential;

a plurality of power-supply lines for supplying the electric power to said active region therethrough, said power-supply lines disposed at different layers of the multilayer wiring structure on said semiconductor substrate and being connected in parallel to each other; and

a common power-supply line provided between said power-supply potential and said active region, the common power-supply line being connected to the power-supply lines and having a current-carrying capacity larger than that of each of the power-supply lines,

wherein said common power-supply line is provided between said active region and said power-supply lines.

Claim 5 (currently amended): A multilayer wiring structure for semiconductor devices, [according to Claim 2,] comprising:

a semiconductor substrate;

at least one active region supplied with an electric power from a power-supply potential;

a plurality of power-supply lines for supplying the electric power to said active region therethrough, said power-supply lines disposed at different layers of the multilayer wiring structure on said semiconductor substrate and being connected in parallel to each other; and

a common power-supply line provided between said power-supply potential and said active region, the common power-supply line being connected to the power-supply lines and having a current-carrying capacity larger than that of each of the power-supply lines,

wherein said common power-supply line is provided between said power-supply potential and said active region, with both ends thereof connecting to the power-supply lines.

Claim 6 (currently amended): A multilayer wiring structure for semiconductor devices, according to Claim [1] 4, wherein said power-supply lines connect in parallel to the active regions.

Claim 7 (currently amended): A multilayer wiring structure for semiconductor devices, according to Claim [1] 4, wherein said power-supply lines connect to said power-supply potential by a plurality of power-supply pads connecting in parallel to said power-supply lines.

Claim 8 (new): A multilayer wiring structure for semiconductor devices, according to Claim 5, wherein said power-supply lines connect in parallel to the active regions.

Claim 9 (new): A multilayer wiring structure for semiconductor devices, according to Claim 5, wherein said power-supply lines connect to said power-supply potential by a plurality of power-supply pads connecting in parallel to said power-supply lines.